What is claimed is:

1. An amplifier circuit comprising:

a) a first transistor having a first base, a first collector and a first emitter;

b) a second transistor having a second base, a second collector and a second emitter, the emitter of the first transistor connected to the base of the second transistor, the collector of the first transistor connected to the collector of the second transistor;

c) a first resistor connected between the collector of the first transistor and the base of the first transistor;

d) a second resistor connected between the base of the first transistor and ground;

e) a first capacitor connected to the base of the first transistor; and

f) a second capacitor connected to the collectors of the first and second transistors, wherein the second capacitor has a capacitance value at least 5 times larger than the first capacitor.

2. The amplifier circuit according to claim 1, wherein the ratio of the capacitance of the first and second capacitors prevents excessive voltage from developing on the collectors of the first and second transistors.

3. The amplifier circuit according to claim 2, wherein the excessive voltage is developed when the circuit is initially powered on.

4. The amplifier circuit according to claim 1, wherein a third resistor is connected between the emitter of the first transistor and ground.

5. The amplifier circuit according to claim 1, wherein a fourth resistor is connected between the emitter of the second transistor and ground.

6. The amplifier circuit according to claim 1, wherein a current source is connected to the collectors of the first and second transistors.

7. The amplifier circuit according to claim 1, wherein a first and second serially connected diode are connected across the first resistor, the first and second diodes preventing excessive voltage from developing on the collector of the first and second transistors.

8. The amplifier circuit according to claim 1, wherein a third transistor is connected across the first resistor, the third transistor preventing excessive voltage from developing on the collector of the first and second transistors.

9. The amplifier circuit according to claim 8, wherein the third transistor has a base, an emitter and a collector, the collector of the third transistor connected to collector of the

first transistor, the emitter of the third transistor connected to the base of the first transistor, the base of the third transistor connected to a parallel combination of a fifth resistor and a sixth resistor, the fifth resistor connected to the collector of the first transistor and the sixth resistor connected to ground.

10. The amplifier circuit according to claim 1, wherein a fourth transistor is connected across the first transistor, the fourth transistor having a base, a collector and an emitter, the collector of the fourth transistor connected to the collector of the first transistor, the emitter of the fourth transistor connected to the emitter of the first transistor, the base of the fourth transistor connected to a combination of a seventh resistor and an eighth resistor, the seventh resistor connected to the collector of the fourth transistor and the eighth resistor connected to ground, the fourth transistor preventing excessive voltage from developing on the collectors of the first and second transistors.

11. An overvoltage protection circuit for an amplifier comprising:

a) a darlington gain block amplifier having an input terminal and an output terminal;

b) a first capacitor connected to the base of the first transistor; and

c) a second capacitor connected to the collectors of the first and second transistors, wherein the second capacitor has a capacitance value greater than the first

capacitor, the larger second capacitor preventing an excessive voltage from developing on the collector of the first transistor during startup.

12. The circuit according to claim 11, wherein the second capacitor has a capacitance value at least 5 times larger than the first capacitor.

13. The circuit according to claim 11, wherein the darlington gain block amplifier includes:

a) a first transistor having a first base, a first collector and a first emitter; and

b) a second transistor having a second base, a second collector and a second emitter, the emitter of the first transistor connected to the base of the second transistor, the collector of the first transistor connected to the collector of the second transistor.

14. An amplifier circuit comprising:

a) a first transistor having a first base, a first collector and a first emitter;

b) a second transistor having a second base, a second collector and a second emitter, the emitter of the first transistor connected to the base of the second transistor, the collector of the first transistor connected to the collector of the second transistor;

c) a first resistor connected between the collector of the first transistor and the base of the first transistor;

d) a second resistor connected between the base of the first transistor and ground;

e) a first capacitor connected to the base of the first transistor;

f) a second capacitor connected to the collectors of the first and second transistors; and

g) two serially connected diodes connected across the first resistor, the diodes preventing excessive voltage from developing on the collector of the first and second transistors.

15. An amplifier circuit comprising:

a) a first transistor having a first base, a first collector and a first emitter;

b) a second transistor having a second base, a second collector and a second emitter, the emitter of the first transistor connected to the base of the second transistor, the collector of the first transistor connected to the collector of the second transistor;

c) a first resistor connected between the collector of the first transistor and the base of the first transistor;

d) a second resistor connected between the base of the first transistor and ground;

e) a first capacitor connected to the base of the first transistor;

f) a second capacitor connected to the collectors of the first and second transistors; and

g) a third transistor connected across the first resistor, the third transistor preventing excessive voltage from developing on the collector of the first and second transistors.

16. The amplifier circuit according to claim 15, wherein the third transistor has a base, an emitter and a collector, the collector of the third transistor connected to the collector of the first transistor, the emitter of the third transistor connected to the base of the first transistor, the base of the third transistor connected to a parallel combination of a fifth resistor and a sixth resistor, the fifth resistor connected to the collector of the first transistor and the sixth resistor connected to ground.

17. An amplifier circuit comprising:

a) a first transistor having a first base, a first collector and a first emitter;

b) a second transistor having a second base, a second collector and a second emitter, the emitter of the first transistor connected to the base of the second transistor, the collector of the first transistor connected to the collector of the second transistor;

c) a first resistor connected between the collector of the first transistor and the base of the first transistor;

d) a second resistor connected between the base of the first transistor and ground;

e) a first capacitor connected to the base of the first transistor;

f) a second capacitor connected to the collectors of the first and second transistors; and

g) a fourth transistor connected across the first transistor, the fourth transistor preventing excessive voltage from developing on the collectors of the first and second transistors.

18. The amplifier circuit according to claim 17, wherein the fourth transistor has a base, a collector and an emitter, the collector of the fourth transistor connected to the collector of the first transistor, the emitter of the fourth transistor connected to the emitter of the first transistor, the base of the fourth transistor connected to a parallel combination of a seventh resistor and an eighth resistor, the seventh resistor connected to the collector of the first transistor and the eighth resistor connected to ground.

19. An overvoltage protection circuit for transistors comprising:

a) a first and second transistor, each transistor having a base, a collector and an emitter, the first and second transistor connected in a darlington configuration;

b) a biasing network coupled to the first and second transistors for supplying a bias voltage to the first and second transistors;

c) a first and second de-coupling capacitor coupled to the first and second transistors; and

d) the second capacitor having a larger capacitance than the first capacitor such that excessive voltage is prevented from developing on the collector of the first and second transistors.

20. The circuit according to claim 19, wherein the second capacitor has a capacitance value at least 5 times larger than the first capacitor.